

**WE CLAIM:**

- 1     1.     An integrated memory, comprising:  
2             a memory cell array, the memory cell array having word lines for the  
3     selection of memory cells and bit lines for reading out or writing data signals of the  
4     memory cells, the bit lines being organized in bit line pairs, the bit lines of one of  
5     the bit line pair crossing one another at a crossing location and running parallel to  
6     one another;  
7             a sense amplifier, which is connected to one of the bit line pairs at one end  
8     of the bit line pair;  
9             two precharge circuits, the precharge circuits being connected to one of the  
10    bit line pairs in order to precharge the bit lines of the bit line pair to a precharge  
11    voltage, one of the precharge circuits being arranged on a side of the crossing  
12    location which faces the sense amplifier, the other of the precharge circuits being  
13    arranged on a side of the crossing location which is remote from the sense  
14    amplifier,  
15             the first precharge circuit facing the sense amplifier being arranged at a  
16    first distance from the crossing location and at a second distance from the sense  
17    amplifier, the first distance being less than the second distance.
- 1     2.     The integrated memory as claimed in claim 1, wherein at least one of the  
2     precharge circuits is arranged within a region, the region being relatively smaller in  
3     relation to the memory cell array and being arranged centrally in relation to the  
4     longitudinal extent of the relevant bit line pair.

1     3.     The integrated memory as claimed in claim 1, wherein at least one of the  
2     precharge circuits has a precharge transistor, the controlled path of the precharge  
3     transistor being connected to a terminal for a supply voltage of the memory and to  
4     one of the bit lines of the respective bit line pair.

1     4.     The integrated memory as claimed in claim 1, wherein at least one of the  
2     precharge circuits has a switch, the bit lines associated with the respective bit line  
3     pair being connected to one another via the switch.

1     5.     A method for operating an integrated memory, the integrated memory  
2     including a memory cell array, the memory cell array having word lines for the  
3     selection of memory cells and bit lines for reading out or writing data signals of the  
4     memory cells, the bit lines being organized in bit line pairs, the bit lines of one of  
5     the bit line pair crossing one another at a crossing location and running parallel to  
6     one another;

7             a sense amplifier, which is connected to one of the bit line pairs at one end  
8     of the bit line pair;

9             two precharge circuits, the precharge circuits being connected to one of the  
10    bit line pairs in order to precharge the bit lines of the bit line pair to a precharge  
11    voltage, one of the precharge circuits being arranged on a side of the crossing  
12    location which faces the sense amplifier, the other of the precharge circuits being  
13    arranged on a side of the crossing location which is remote from the sense  
14    amplifier, the first precharge circuit facing the sense amplifier being arranged at a

15 first distance from the crossing location and at a second distance from the sense  
16 amplifier, the first distance being less than the second distance, comprising:  
17 activating one of the word lines at the beginning of a memory access to  
18 select one of the memory cells;  
19 passing the charge stored in one of the memory cells to one of the bit lines;  
20 passing the charge from the last line to the sense amplifier, which spreads  
21 the respective bit lines;  
22 writing back the signal stored in one of the memory cells to one of the  
23 memory cells again; and  
24 activating a control line for driving one of the precharge circuits, after the  
25 deactivation of one of the word lines, so that the bit lines of a bit line pair are  
26 short-circuited and precharged.

1 6. The integrated memory as claimed in claim 5, wherein at least one of the  
2 precharge circuits is arranged within a region, the region being relatively smaller in  
3 relation to the memory cell array and being arranged centrally in relation to the  
4 longitudinal extent of the relevant bit line pair.

1 7. The integrated memory as claimed in claim 5, wherein at least one of  
2 the precharge circuits has a precharge transistor, the controlled path of the  
3 precharge transistor being connected to a terminal for a supply voltage of the  
4 memory and to one of the bit lines of the respective bit line pair.

1 8. The integrated memory as claimed in claim 5,

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- 2 wherein at least one of the precharge circuits has a switch, the bit lines associated
- 3 with the respective bit line pair being connected to one another via the switch.